Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**Source**

**Gate**

**.087”**

**.067”**

**Top Material: Al**

**Backside Material: Si**

**Gate = .017” X .025”**

**Source = .018” X .024”**

**Mask Ref: HEX-1, GEN 3**

**APPROVED BY: DK DIE SIZE .067” X .087” DATE: 7/11/22**

**MFG: INT’L RECTIFIER THICKNESS .020” P/N: IRFC210**

**DG 10.1.2**

#### Rev B, 7/19/02